Silicon Based Packaging for 400/800/1600 Gb/s Optical Interconnects

The Low Cost Solution for Parallel Optical Interconnects Into the Terabit per Second Age

White Paper

PhotonX Networks

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Executive Summary

Exponential demand for interconnect bandwidth will see data center links running at 400Gb/sec in the near future. Hot on their tails are the anticipated 800 and 1.6Tb/sec links based on either 28 Gbaud-PAM4 or the more future looking 56 Gbaud-PAM4 base rates. Current pluggable module solutions are quickly running out of steam as is evident from the recent annoucement of the COBO specification. How can these complicated and massive interconnect solutions scale to support such massive data loads?

The solution is a novel integration platform developed by PhotonX Networks. A wafer scale packaging solution for surface normal Multi-mode light emitters and detectors, which enable a leap forward in bandwidth density at significant lower cost and dramatically simplifies the challenge of scaling to 800,1600 Gb/sec and beyond.

Introduction

Data centers have seen exponential growth over the past two decades. Modern data centers host many tens of thousands of servers interconnected with an optical network. While these servers are becoming ever more powerful due to rapid developments in CPU & memory technologies, the main bottleneck in data center performance is becoming the available network bandwidth. Servers are continuously processing data at higher rates necessitating faster transport of data between servers. This puts very stringent demands on the interconnect technology and the design of the switching fabrics. As interconnect technology becomes more and more complex to implement, the price associated with adopting and deploying it grows out of proportion when compared to the cost of compute. Today the bill of materials (BOM) for a high end Ethernet switch in a data center is dominated (>50%) by the cost of the optical interconnect modules. More than that, the power consumption of optical interconnects, at ever increasing bit rates, is also beginning to dominate the total power consumption. At bit rates of 25 Gbaud and beyond, as is proposed for next generation switch fabrics, additional circuitry would be needed to support the connections between switching ASICs and interconnect modules. Current interconnect modules on their own will require >100 Watts. Looking forwards to emerging signaling rates of 25Gbaud (& 50 Gbaud) requiring the inclusion of additional regeneration and clock recovery power consumption is expected to exceed >200 Watts which makes the interconnect consume ~50% of power used by such a switch. It is clear that a new paradigm is needed to solve the interconnect challenges facing data center network builders and operators.

PhotonX Networks, a spin-off of the Eindhoven University of Technology, is commercializing a novel and unique solution that will revolutionize the way high capacity parallel optical interconnects are fabricated. By using proprietary technology, already used to demonstrate state-of-the-art 200Gb/sec SR-8 optical engines[1] a low cost and wafer scale packaging solution has been developed which allows co-integration of more than 40 separate optical channels with easy direct cable attached optical interfacing. The critical components are interconnected using carefully designed metallic waveguides to insure optimal signal integrity which has been tested to support 28 Gbaud-PAM4 signaling and possesses a 3dB bandwidth >40GHz.

[1] C. Li, O. Raz, F. Kraemer, R. Stabile,"Silicon Interposer Based QSFP-DD Transceiver Demonstrator with >10 Gbps/mm2 Bandwidth Density", proc. Of European Conference on Optical Communications 2018, Rome, Italy

Technology breakthrough

Optical interconnects, a key component in the DCN (Data Center Network), have been developed and deployed by using different approaches. PhotonX networks, building on the advanced prototyping activities at Eindhoven University of Technology, is pioneering a novel packaging solution for parallel optical interconnects.
The solution is based on the use of silicon wafers as a packaging platform for surface normal lasers (vertical cavity surface emitting lasers or VCSELs for short) and detectors which are commonly deployed in short reach data center interconnects today. VCSELs are today the most efficient, lowest cost, and most widely used laser source for interconnects due to their low threshold current, small size, direct modulation and wafer level testing capabilities, as well as their ability to be integrated in multi-component arrays. VCSELs have prevailed in short reach (up to hundreds of meters) interconnects using MM fiber and operating at 850 nm. VCSELs may also find applications for communication over longer distances in data centers if maturity of long wavelength VCSELs and high volume production becomes a reality. High speed VCSELs at 1550 nm have already been shown enabling data transmission at bit rates up to 35 Gb/s in data communication applications.

As VCSELs lend themselves easily to production in arrays (1D and 2D), they have found many applications in parallel optical interconnect solutions. The main challenge for parallel optical transceiver design is the packaging of the components. Over the years different substrates have been put forward for the packaging of VCSEL's based interconnects among which: printed and flexible circuit boards, glass and ceramics. More recently there is increased interest in the use of silicon wafers for such packaging solutions.
Table 1 summarizes the main attributes of using the different packaging platforms.

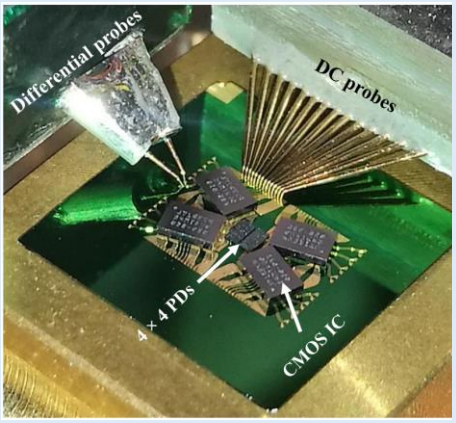
Will Silicon Photonics solve the interconnect problem?
SiPh devices are mostly fabricated on silicon on insulator (SOI) platforms. SOI wafers are composed of a high quality crystalline silicon layer over a buried silicon dioxide (SiO2) layer and a bulk silicon support layer. The top silicon layer can be used to fabricate optical waveguides and devices, because the buried SiO2 enables light propagation on the basis of total internal reflection on the top Si layer. Data center optical interconnects based on SiPh are beginning to emerge with an anticipated sweet spot at 100Gb/sec (QSFP28) for 500-2000 meters transmission distances. Both parallel single mode (PSM) and coarse wavelength division multiplexing (CWDM) have been commercialized.
However, because of the lack of silicon light sources a SiPh solution is always dependent on an external light source. This greatly complicates the packaging of SiPh transceivers and leads to higher costs and increased power consumption.

Table 1. Comparison of different packaging substrates for parallel optical interconnects

Properties	PCB	FPC	GLASS	CERAMIC	SILICON
Cost	Very low	Low	Low	Moderate	Low
Obtainable resolution [micron]	>150	>50	>1	>10	>1
Thermal conduction	Poor	Poor	Poor	Good	Excellent
Frequency range [GHz]	<10GHz	<25GHz	>25GHz	>25GHz	>25GHz

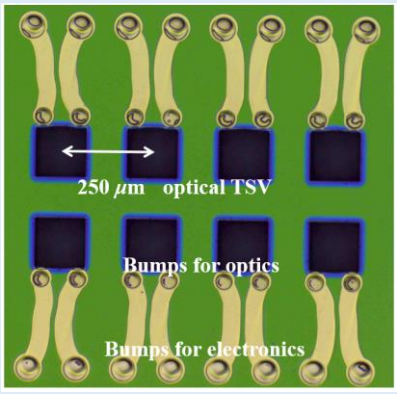
Technology demonstrators

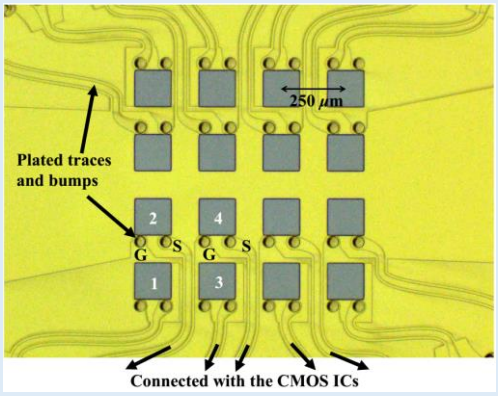
In the figure on the left we show an image of a fully assembled 200Gb/sec optical engine based on arrays of 8x25 Gb/sec VCSEL lasers and 8x25 Gb/sec surface normal photo detectors. The module is shown under testing and performance obtained exceeds that of a commercial module.



A 200 Gb/sec prototype optical engine under testing. Whole assembly measures ~6x6 mm leading to a bandwidth density higher than 10 Gb/sec/mm²

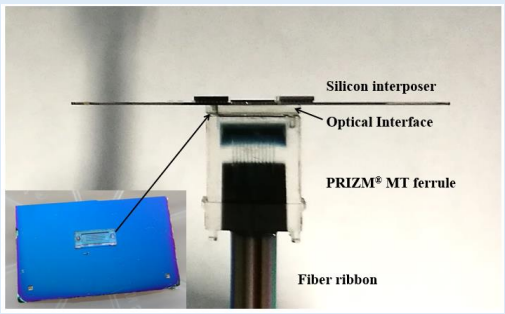
The improved performance is driven by the choice of substrate and the careful design of very short metallic connections between the ICs and the opto-electronic devices. As can be seen in the image below the required metallic connections can be made as short as a few hundreds of microns. Also clearly visible in the image are the gold bumps which are lithographically deposited on the interposer (saving the cost and time of stud bumping the entire wafer) and the optical through holes which are being formed in the process. For devices with an increased number of ports, the same lithographic process can be used to create several rows of emitters/detectors as was used for the 200 Gb/sec engine example without loss of performance, thanks to our clever design methodology.





Two lay-outs of metallic interconnect highlighting the versatility of the PhotonX packaging concept

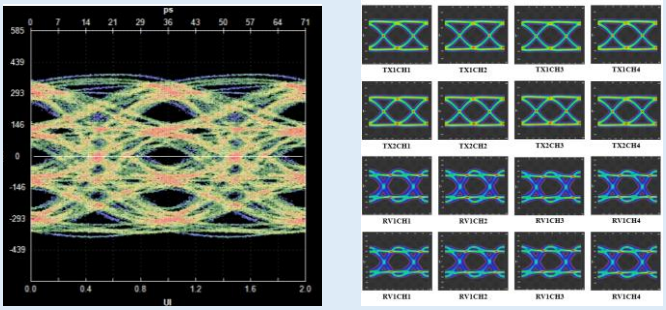
To complement the electronic part of the solution, a low cost optical interface has been designed and tested based on a collimated MPO connector, modified to directly interface with our optical engine. A side view of the interposer with MPO connector attached in shown below. Obtained insertion loss is ~1dB which is mostly due to collimating loss and not coupling between light emitters/detectors and lenses array.



Two lay-outs of metallic interconnect highlighting the versatility of the PhotonX packaging concept

Technology performance

The integrated components show excellent performance under testing. Error free operation is easily obtained with performance equivalent of better than commercial devices. The performance of the interconnecting metallic wires has also been characterized beyond the tested performance of the fully integrated module. 28 Gbaud – PAM4 signaling has been successfully transmitted without any distortion over up to 5 mm of transmission lines on the processed interposer. Measured 8x25 Gb/sec Tx and Rx eye patterns, also show exceptional jitter free operation even when CDR functionality inside TIA CMOS ICs has been switched off!



28 Gbaud PAM-4 eye patterns and 8x25 Gb/sec NRZ Tx and Rx eye patterns

Technology potential

The PhotonX technology has been developed in close collaboration with the Technical University of Eindhoven in The Netherlands. The underlying processes and concept collimating in the demonstrators have been patented. As switching ASICs move towards signaling at 50 Gbaud (NRZ and/or PAM-4) the packaging challenges facing traditional techniques are only getting bigger. The PhotonX technology has proven its resilience at ever increasing rates and channel numbers[2]. The further increase in the number of channels and single channel speed is actively being pursued. In addition, the potential of combining the technology with silicon photonics is being evaluated

Summary

The challenges facing manufacturers of optical interconnect modules are putting an increasing strain on the traditional packaging techniques used by the industry. In order to meet the demand for more optical channels running at ever higher speeds, a new packaging technology is needed. PhotonX Networks is introducing a novel packaging solution which has been proven through multiple demonstrators to provide scalability in both number of channel and channel bit rates as well as drastically reduce the cost of packaging.

For more info contact us at info@photonxnetworks.com

2 C. Li , X. Zhang, T. Li , O. Raz , R. Stabile, “48-Channel Matrix Optical Transmitter on a Single Direct Fiber Connector”, IEEE TRANSACTIONS ON ELECTRON DEVICES, 2018